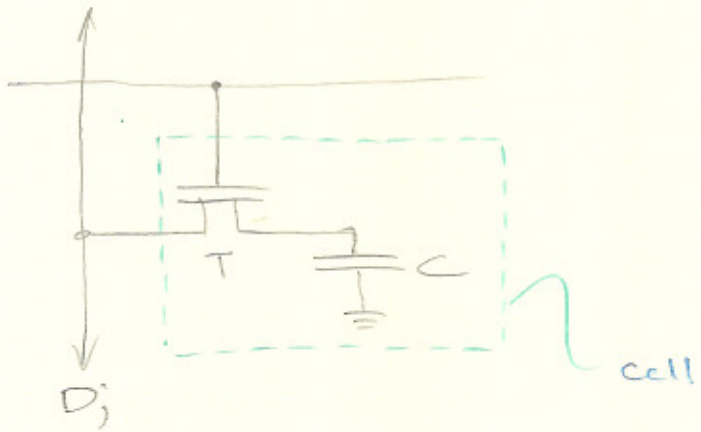
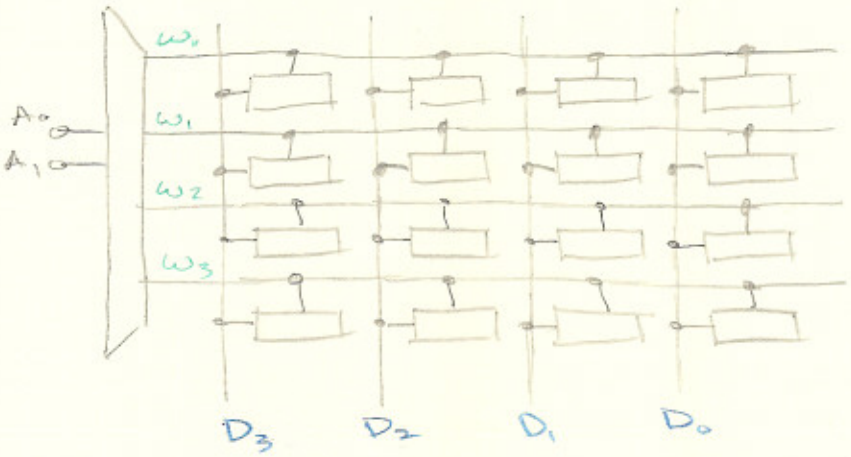
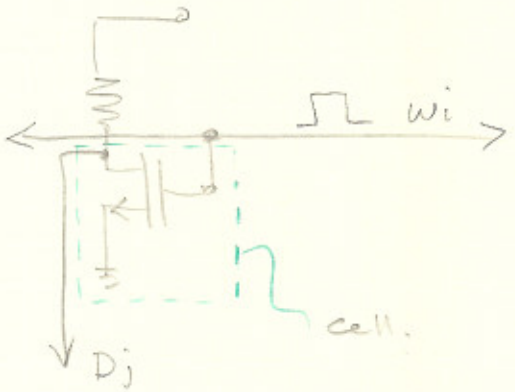
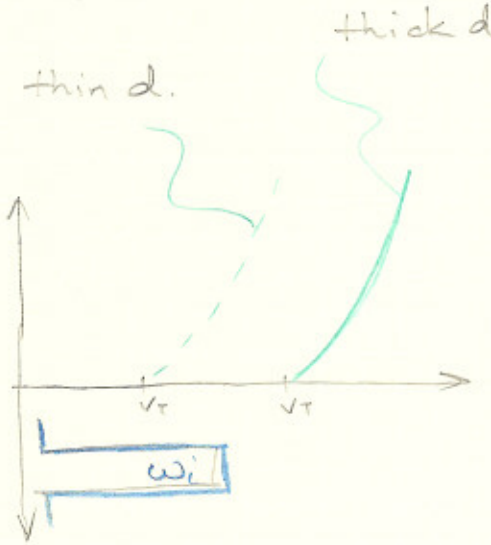
Dynamic RAM

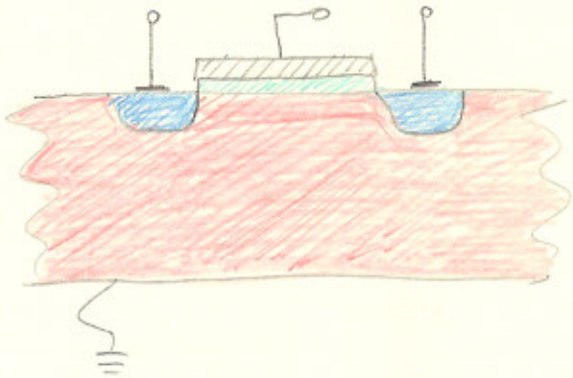




ROM







$\downarrow d$
$\uparrow$

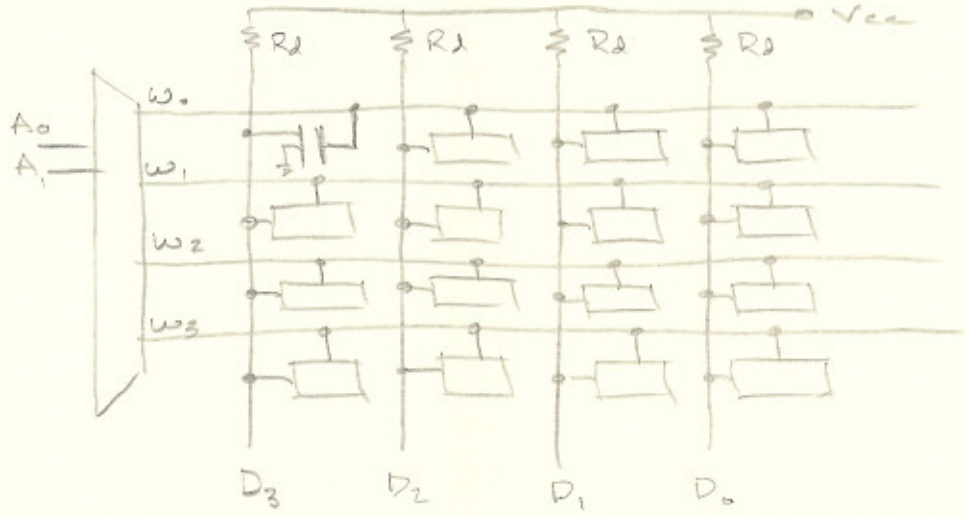
$$\mathcal{E}_T = \frac{V_{dsT}}{d}$$

$$d \uparrow \Rightarrow \quad \mathcal{E}_T \downarrow$$

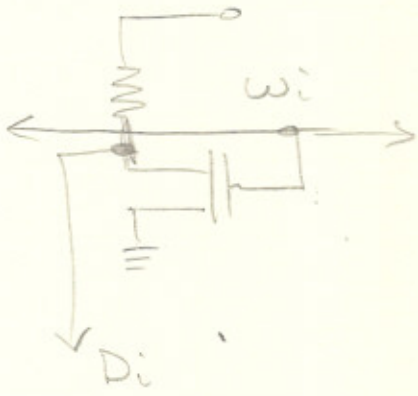
by increasing the thickness of the silicon oxide we increase the electric field strength required to activate the transistor.

Hence, if we want to store a zero, then we make d thin. If we want a logical one, then we should make d thick.

However, here only the chip producer can store information.



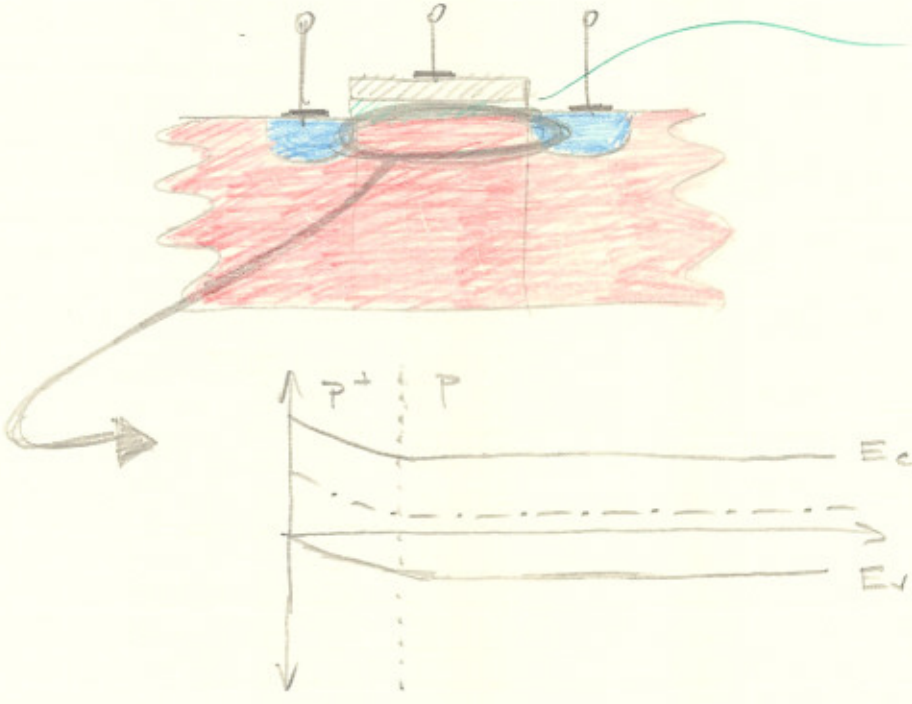
PROM



If the grid starts out all low. And if we apply a neg voltage on Dj and high voltage on Wi.

We destroy the transistor (Burn it) so that this transistor now emitts a low.

EPROM



the silicon layer is made up of Si_4N_3 and SiO_2

If by making the p^+ substrate more plus so that it it is p^{++}, we will increase the treshold voltage of the transistor.

But putting a large voltage on the gate electrons are pulled from the P type material into the silicon. UV light can be used to remove these electrons. This changing of electrons shifts the voltage threshold.